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OKI.

IN THE UNITED STATE PATENT AND TRADEMARK OFFICE

In re Patent application of :

[inventor] :

[Serial No.] :

[Filed] :

[TITLE OF THE INVENTION]

SUBMISSION OF ENGLISH-LANGUAGE TRANSLATION OF FOREIGN-LANGUAGE PROVISIONAL APPLICATION

Honorable Commissioner For Patents
Washington, D.C. 20231

Sir:

I, Yukie SATO, declare and say:
(print name of translator)

that I am conversant in both the Japanese and English languages;

that I am presently engaged as a translator in these languages;

that the attached document represents an accurate English-language translation of the U.S Provisional Application Serial [60/413,753], filed September 27, 2002].

Signed this 20th day of May, 2003.

Yukie Sato
(signature of translator)

provisional

F-01ED0520

VOLTAGE LEVEL SHIFTING CIRCUIT

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a voltage level shifting circuit for outputting signals outputted from a circuit operating at a low power supply voltage to a circuit operating at a high power supply voltage. The invention relates particularly to a voltage level shifting circuit suitable for a drive circuit for driving a vacuum fluorescent display and a drive circuit for driving an LCD panel.

DESCRIPTION OF THE RELATED ART

For example, there is United States Patent No. 5,113,097 (Lee) as a technique related to the invention. In Fig. 4 of Lee, a level shifting circuit is disclosed in which an input signal Vin having the logic levels of 0 v (Vss1) and 15 v (+VDD) is converted to an output signal Vout having the logic levels of -5 v (-Vss2) and 15 v (+VDD). More specifically, Lee discloses that a signal having a relatively small logical amplitude is converted to a signal having a relatively large logical amplitude.

Referring to Fig. 4 of Lee, a PMOS transistor 206 and a PMOS transistor 208 having a gate electrode for receiving the input signal Vin having a small logical amplitude are

connected between a power supply +VDD and a power supply -Vss2. The difference between the potential level of the power supply +VDD and the potential level of a power supply Vss1 is 15 v. On the other hand, the difference between the potential level of the power supply +VDD and the potential level of the power supply -Vss2 is 20 v, and this value is greater than the difference between the potential level of the power supply +VDD and the potential level of the power supply Vss1. Therefore, the withstand voltages of the PMOS transistor 206 and the PMOS transistor 208 are required to be higher than the withstand voltages of MOS transistors configuring an inverter 404 and an inverter 202. (To simplify the description, a transistor having a low withstand voltage is referred to as a low withstand voltage transistor, and a transistor having a high withstand voltage is referred to as a high withstand voltage transistor in the subsequent description). By the same reason, a PMOS transistor 408, an NMOS transistor 210, an NMOS transistor 212 and an NMOS transistor 410 are configured of the high withstand voltage transistors, and each of the transistors configuring the inverter 404 and the inverter 202 is configured of the low withstand voltage transistor.

When the gate-to-source voltages are set to the same value, it is generally known that the current supply capability of the high withstand voltage transistor is lower than the current supply capability of the low withstand voltage

transistor. Fig. 1 is a diagram illustrating the difference between the current supply capability of the high withstand voltage transistor and the current supply capability of the low withstand voltage transistor. In Fig. 1, NMOS transistors where the gate-to-source voltage Vgs is set to 5 v are described as one example. L denotes the gate length of the transistor, and W denotes the gate width of the transistor. IDS denotes the drain-to-source current, and VDS denotes the drain-to-source voltage. The example of Fig. 1 shows that the low withstand voltage transistor can carry a current of 3.0 mA at a drain-to-source voltage of 1.0 v, whereas the high withstand voltage transistor can carry only a current of 500 μA. This means that the transistor size (transistor dimensions) is needs to be set about six times the transistor size of the low withstand voltage transistor in order to equalize the current supply capability of the high withstand voltage transistor with the current supply capability of the low withstand voltage transistor. The current supply capability also relates to the operating speed of the transistor. This also means that the transistor size (transistor dimensions) needs to be set about six times the transistor size of the low withstand voltage transistor in order to equalize the operating speed of the high withstand voltage transistor with the operating speed of the low withstand voltage transistor.

For the drive circuit for driving the vacuum fluorescent

display and the drive circuit for driving the LCD panel, the number of the voltage level shifting circuits is required to meet the number of display devices, ranging from a few tens to a few hundreds of the circuits. Thus, when the voltage level shifting circuit of the configuration described above is simply adapted to the drive circuit, an area for forming the drive circuit on a chip is likely to be expanded in order to further increase the operating speed of the drive circuit. Alternatively, it is likely to be difficult to increase the operating speed of the drive circuit in order to further reduce the area for forming the drive circuit on the chip, or to maintain the area on the chip. Therefore, a voltage level shifting circuit having an improved operating speed and an improved area for forming the circuit is desired.

SUMMARY OF THE INVENTION

The invention has been made in consideration of the points to be improved. The following are the outlines of a typical voltage level shifting circuit in the invention disclosed in the application. That is, a voltage level shifting circuit has: a first power supply node applied with a first power supply potential level; a second power supply node applied with a second power supply potential level higher than the first power supply potential level; and a third power supply node applied with a third power supply potential level

higher than the second power supply potential level. The voltage level shifting circuit further has: a signal input circuit connected between the first power supply node and the second power supply node, the signal input circuit for receiving a signal having the first power supply potential level and the second power supply potential level, and outputting a complementary signal having the first power supply potential level and the second power supply potential level; and a complementary signal input circuit connected to the first power supply node, the complementary signal input circuit having a first electrode connected to the first power supply node, a second electrode, and a gate electrode for receiving the complementary signal, and including a pair of first MOS transistors having a first withstand voltage. The voltage level shifting circuit further has: a load circuit connected to the third power supply node, the load circuit having a first electrode connected to the third power supply node, a second electrode, and a gate electrode, and including a pair of second MOS transistors having a second withstand voltage greater than the first withstand voltage; and a first voltage reducing device connected between the load circuit and the complementary signal input circuit, the first voltage reducing device for preventing a potential exceeding the first withstand voltage from being fed to the complementary signal input circuit. The voltage level shifting circuit further has: a third MOS

transistor connected between the third power supply node and an output node, the third MOS transistor having the second withstand voltage for electrically connecting the third power supply potential node to the output node in response to a potential level outputted from the load circuit; a fourth MOS transistor connected between the first power supply node and the output node, the fourth MOS transistor having the first withstand voltage for electrically connecting the first power supply potential node to the output node in response to a potential level of one of signals configuring the complementary signal; and a second voltage reducing device connected between the third MOS transistor and the fourth MOS transistor, the second voltage reducing device for preventing a potential exceeding the first withstand voltage from being fed to the fourth MOS transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram illustrating the difference between the current supply capability of the high withstand voltage transistor and the current supply capability of the low withstand voltage transistor;

Fig. 2 is a circuit diagram illustrating a voltage level shifting circuit 200 of a first embodiment according to the invention; and

Fig. 3 is a circuit diagram illustrating a voltage level

shifting circuit 300 of a second embodiment according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereafter, embodiments of the invention will be described in detail with reference to the drawings.

In order to facilitate the description, the same components are designated the same numerals and signs, omitting the overlapping description.

First Embodiment

Fig. 2 is a circuit diagram illustrating a voltage level shifting circuit 200 of a first embodiment according to the invention.

The voltage level shifting circuit 200 is formed on a semiconductor substrate, which is mainly configured of a signal input part 201, a level shift part 203, and a signal output part 205.

The signal input part 201 has an inverter 207 and an inverter 209 to which a power supply potential VDD and a ground potential VSS are applied. The level of the power supply potential VDD is 5 v, for example, being set to a level lower than the level of a power supply potential VPP, which will be described later. The level of the ground potential VSS is 0 v, for example. The inverter 207 and the inverter 209 are

configured of a well-known CMOS inverter. A signal applied to an input terminal IN which is output from an internal circuit, not shown, has an amplitude between the power supply potential VDD and the ground potential VSS. (To facilitate the description, this amplitude is referred to as a first amplitude.) In other words, a high level of the signal applied to the input terminal IN is about 5 v, and a low level is about 0 v. The inverter 207 and the inverter 209 input a signal having the first amplitude and output the signal having the first amplitude. Since only a relatively low voltage (about 5 v at the maximum) is applied to drain electrodes of MOS transistors configuring the inverter 207 and the inverter 209, these transistors are not required to have so high withstand voltage characteristics. Thus, the transistors are formed in a low withstand voltage area LV as low withstand voltage transistors. Since the operating speed of the low withstand voltage transistor is faster than the operating speed of the high withstand voltage transistor, the signal having the first amplitude applied to the input terminal IN is transferred to the level shift part 203 in the subsequent stage at high speed. Because the low withstand voltage transistor can be formed of a transistor having a relatively short gate length and a narrow gate width, the area occupied by the signal input part 201 is relatively small on the semiconductor substrate.

The level shift part 203 has a PMOS transistor 211, a

PMOS transistor 213, an NMOS transistor 215, an NMOS transistor 217, an NMOS transistor 219, and an NMOS transistor 221, which are disposed between the power supply potential VPP and ground potential VSS. The level of the power supply potential VPP is 20 v, for example, being set to a level higher than the level of a power supply potential VDD. The level of the ground potential VSS is 0 v, for example.

The PMOS transistor 211, the PMOS transistor 213, the NMOS transistor 215, and the NMOS transistor 217 configure a current mirror type differential amplifier circuit.

The PMOS transistor 211 has a source electrode connected to the power supply potential VPP, a drain electrode and a gate electrode connected to a drain electrode of the NMOS transistor 219. The PMOS transistor 213 has a source electrode connected to the power supply potential VPP, a drain electrode connected to the drain electrode of NMOS transistor 221, and a gate electrode connected to the gate electrode of the PMOS transistor 211. The PMOS transistor 211 and the PMOS transistor 213 configure a current mirror type load circuit.

The NMOS transistor 215 has a source electrode connected to the ground potential VSS, a drain electrode connected to a source electrode of the NMOS transistor 219, and a gate electrode connected to an output terminal of the inverter 209. The NMOS transistor 217 has a source electrode connected to the ground potential VSS, a drain electrode connected to a

source electrode of the NMOS transistor 221, and a gate electrode connected to an output terminal of the inverter 207. The NMOS transistor 215 and the NMOS transistor 217 configure a pair of signal input transistors of a differential amplifier circuit.

The NMOS transistor 219 has the source electrode connected to the drain electrode of the PMOS transistor 211, the drain electrode connected to the drain electrode of the NMOS transistor 215, and a gate electrode connected to the power supply potential VDD. The NMOS transistor 221 has the source electrode connected to the drain electrode of the PMOS transistor 213, the drain electrode connected to the drain electrode of the NMOS transistor 217, and a gate electrode connected to the power supply potential VDD. The NMOS transistor 219 and the NMOS transistor 221 connected between the current mirror type load circuit and the pair of signal input transistors, which configure a voltage relaxation device (voltage reducing device) for relaxing (reducing) a voltage applied to the drain electrodes of the pair of signal input transistors.

Since a relatively high voltage (about 20 v at the maximum) is applied to the drain electrodes of the NMOS transistor 211, the NMOS transistor 213, the NMOS transistor 219, and the NMOS transistor 221, the transistors are required to have high withstand voltage characteristics. Therefore,

the transistors are formed in a high withstand voltage area HV as high withstand voltage transistors.

To the gate electrode of the NMOS transistor 219, the power supply potential VDD (5 v) at a level lower than the level of the power supply potential VPP (20 v). Thus, although a relatively high voltage (voltage nearly 20 v) is applied to the drain electrode of the NMOS transistor 219, the voltage applied to the drain electrode itself does not appear in the source electrode thereof. More specifically, (VDD - Vtn) is applied to the source electrode of the NMOS transistor 219, where Vtn denotes the threshold voltage of the NMOS transistor 219, and the value is about 1 v. Consequently, only a relatively low voltage of about 4 v is applied to the drain electrode of the NMOS transistor 215 at the maximum. Similarly, the power supply potential VDD (5 v) at a level lower than the level of the power supply potential VPP (20 v) is applied to the gate electrode of the NMOS transistor 221. Therefore, although a relatively high voltage (voltage nearly 20 v) is applied to the drain electrode of the NMOS transistor 221, the voltage applied to the drain electrode itself does not appear in the source electrode thereof. More specifically, (VDD - Vtn) is applied to the source electrode of the NMOS transistor 217, where Vtn denotes the threshold voltage of the NMOS transistor 221, and the value is about 1 v. Consequently, only a relatively low voltage of about 4 v is applied to the drain

electrode of the NMOS transistor 217 at the maximum.

Since only a relatively low voltage (about 4 v at the maximum) is applied to the drain electrodes of the NMOS transistor 215 and the NMOS transistor 217, the transistors are not required to have high withstand voltage characteristics. Therefore, the transistors are formed in the low withstand voltage area LV as low withstand voltage transistors. Since the operating speed of the low withstand voltage transistor is faster than the operating speed of the high withstand voltage transistor, the signal having the first amplitude outputted from the signal input part 201 can operate the differential amplifier circuit at high speed. That is, the level of the drain electrode of the PMOS transistor 213 can be determined at high speed, which is the output of the level shift part 203.

When the high withstand voltage transistors are used for the NMOS transistor 215 and the NMOS transistor 217 to obtain the current supply capability equal to the case where the low withstand voltage transistors are used for the NMOS transistor 215 and the NMOS transistor 217, the required area on the semiconductor substrate is about six times that in the case where the low withstand voltage transistors are used for the NMOS transistor 215 and the NMOS transistor 217. Therefore, even though two high withstand voltage transistors are added as a voltage relaxation device (voltage reducing device), the area occupied by the level shift part 203 can be reduced on

the semiconductor substrate without decreasing the operating speed.

The signal output part 205 has a PMOS transistor 223, a PMOS transistor 225, and an NMOS transistor 227 disposed between the power supply potential VPP and a ground potential VSS. The signal output part 205 outputs a signal having a second amplitude where the power supply potential VPP is set to a logic high level, and the ground potential VSS is set to a logic low level.

The PMOS transistor 223 has a source electrode connected to the power supply potential VPP, a drain electrode connected to an output terminal OUT, and a gate electrode connected to the drain electrode of the PMOS transistor 213. The NMOS transistor 225 has a source electrode connected to the ground potential VSS, a drain electrode connected to a drain electrode of the NMOS transistor 227, and a gate electrode connected to the output terminal of the inverter 209. The PMOS transistor 223 is a charge transistor for applying the power supply potential VPP to a load, not shown, connected to the output terminal OUT. The NMOS transistor 225 is a discharge transistor for applying the power supply potential VSS to the load connected to the output terminal OUT.

The NMOS transistor 227 has a source electrode connected to the output terminal OUT, the drain electrode connected to the drain electrode of the NMOS transistor 225, and a gate

electrode connected to the power supply potential VDD. The NMOS transistor 227 configures a voltage relaxation device (voltage reducing device) for relaxing (reducing) a voltage applied to the drain electrode of the NMOS transistor 225.

Since a relatively high voltage (about 20 v at the maximum) is applied to the drain electrode of the NMOS transistor 223, the transistor is required to have high withstand voltage characteristics. Therefore, the transistor is formed in the high withstand voltage area HV as a high withstand voltage transistor.

To the gate electrode of the NMOS transistor 227, the power supply potential VDD (5 v) at a level lower than the level of the power supply potential VPP (20 v) is applied. Therefore, although a relatively high voltage (voltage nearly 20 v) is applied to the drain electrode of the NMOS transistor 227, the voltage applied to the drain electrode itself does not appear in the source electrode thereof. More specifically, (VDD - Vtn) is applied to the source electrode of the NMOS transistor 227, where Vtn denotes the threshold voltage of the NMOS transistor 227, and the value is about 1 v. Consequently, only a relatively low voltage of about 4 v is applied to the drain electrode of the NMOS transistor 225 at the maximum.

Since only a relatively low voltage (about 4 v at the maximum) is applied to the drain electrode of the NOMS transistor 225, the transistor is not required to have high

withstand voltage characteristics. Therefore, these transistors are formed in the low withstand voltage area LV as low withstand voltage transistors. Since the operating speed of the low withstand voltage transistor is faster than the operating speed of the high withstand voltage transistor, the signal having the first amplitude outputted from the inverter 209 allows the NMOS transistor 225 to be conductive at high speed. That is, low-level output of the signal output part 205 is determined at high speed.

Next, the operation of the voltage level shifting circuit shown in Fig. 2 will be described.

To the input terminal IN, an input signal having logical amplitudes of 0 v (ground potential VSS) and 5 v (power supply potential VDD) is applied from an internal circuit, not shown. The input signal of 0 v indicates a logic low level, and the input signal of 5 v indicates a logic high level.

When the high-level input signal (5 v) is applied to the input terminal IN, the inverter 207 outputs a low-level signal (0 v). The inverter 209 receives the low-level signal and outputs high-level signal (5 v).

When the NMOS transistor 215 receives the high-level signal, it is turned to an ON state. When the NMOS transistor 215 is in the ON state, a first current path from the power supply potential VPP to the ground potential VSS is conductive, the first current path is formed of the PMOS transistor 211,

the NMOS transistor 219 and the NMOS transistor 215.

More specifically, the NMOS transistor 215 is turned to the ON state, and then the potentials of node A and node B drop toward 0 v. The drain-to-source voltage of the NMOS transistor 219 is set to have a size where the NMOS transistor 219 operates in a saturation region. Thus, the potential of the node A is a level that the drain-to-source voltage Vds of the NMOS transistor 219 is added to the potential of the node B. When the potential of the node A is turned toward 0 v, the PMOS transistor 211 is turned to an ON state. The PMOS transistor 211 in the ON state carries current through the first current path from the power supply potential VPP to the ground potential VSS. However, a limit is imposed in the current carried through the first current path from the power supply potential VPP to the ground potential VSS by the NMOS transistor 219 operating in the saturation region. More specifically, a predetermined amount of current determined by the NMOS transistor 219 is carried through the first current path as long as the signal level applied to the input terminal IN is at high level, but current equal to or greater than the drain-to-source current determined by the NMOS transistor 219 is not carried through the first current path. Accordingly, current consumption is not increased largely.

Since the PMOS transistor 211 configures the current mirror circuit with the PMOS transistor 213, the PMOS

transistor 211 is tuned to the ON state to cause the PMOS transistor 213 to be turned to an ON state. The PMOS transistor 213 in the ON state is about to carry current through a second current path from the power supply potential VPP to the ground potential VSS.

On the other hand, the NMOS transistor 217 is in an OFF state because it receives a low-level signal. When the NMOS transistor 217 is in the OFF state, the second current path from the power supply potential VPP to the ground potential VSS is interrupted, the second current path is formed of the PMOS transistor 213, the NMOS transistor 221, and the NMOS transistor 217.

More specifically, the NMOS transistor 217 is turned to the OFF state, and then the potentials of node C and node D are about to increase toward 20 v. Since only 5 v is applied to the gate electrode of the NMOS transistor 221, the potential of the node D drops to about 4 v (5 v - 1 v), not reaching 20 v. The potential of the node C is turned to about 20 v by the PMOS transistor 213 in the ON state.

When the potential of the node C is turned to 20 v, the PMOS transistor 223 is turned to an OFF state. The PMOS transistor 223 in the OFF state turns the PMOS transistor 223 in the signal output part 205 to be an OFF state.

Since the NMOS transistor 225 in the signal output part 205 receives a high-level signal, it is turned to an ON state.

The NMOS transistor 225 is in the ON state, and then the potential of node E drops toward 0 v. Consequently, charge of the load, not shown, connected to the output terminal OUT is discharged by the NMOS transistor 225.

Next, when a low-level input signal (0 v) is applied to the input terminal IN, the inverter 207 outputs a high-level signal (5 v). The inverter 209 receives the high-level signal and outputs a low-level signal (0 v).

Since the NMOS transistor 215 receives the low-level signal, it is turned to an OFF state. When the NMOS transistor 215 is in the OFF state, the first current path is interrupted.

More specifically, the NMOS transistor 215 is turned to the OFF state, and then the potentials of the node A and node B increase toward 20 v. Since only 5 v is applied to the gate electrode of the NMOS transistor 219, the potential of the node B drops to about 4 v (5 v - 1 v), not reaching 20 v.

Since the potential of the node A increases to about 20 v, the PMOS transistor 211 is turned to an OFF state. Because the PMOS transistor 213 and the PMOS transistor 211 form the current mirror circuit, the PMOS transistor 211 is turned to the OFF state, and then the PMOS transistor 213 is also turned to an OFF state.

On the other hand, since the NMOS transistor 217 receives a high-level signal, it is turned to an ON state. The NMOS transistor 217 is turned to the ON state, and then the potential

of the node D drops toward 0 v. Consequently, the potential of the node C drops to 0 v.

When the potential of the node C is turned to 0 v, the PMOS transistor 223 in the signal output part 205 is turned to an ON state. In the meantime, since the NMOS transistor 225 receives a low-level signal, it is turned to an OFF state. Thus, the PMOS transistor 223 outputs the power supply potential VPP to the output terminal OUT. Therefore, the load, not shown, connected to the output terminal OUT is charged by the PMOS transistor 223.

At this time, the potential of the node E is about to increase toward 20 v. However, because only 5 v is applied to the gate electrode of the NMOS transistor 227, the potential of node E increase to only about 4 v (5 v - 1 v), not reaching 20 v.

As it can be understood from the operation described above, the voltage level shifting circuit 200 has the function of converting the signal having the first amplitude to the signal having the second amplitude greater than the first amplitude for output.

As described above, in the voltage level shifting circuit of the first embodiment, the pair of signal input transistors (the NMOS transistor 215 and the NMOS transistor 217, for example) and the discharge transistor in the output circuit part (the NMOS transistor 225, for example), each of which

receives the signal having the first amplitude relatively small, are configured of the low withstand voltage transistors. Therefore, a voltage level shifting circuit having a further improved operating speed can be provided. Furthermore, a voltage level shifting circuit capable of reducing the area for forming the circuits can be provided as the operating speed is maintained.

In addition, in the voltage level shifting circuit of the first embodiment, the example is described as an instance that the level of the ground potential VSS is 0 v. However, the potential applied to the ground potential VSS (potential applied to the sources of the NMOS transistor 215, the NMOS transistor 217, and the NMOS transistor 225) may be negative potential as long as the potential is that allows the MOS transistors to be turned to the OFF state.

In the voltage level shifting circuit of the first embodiment, the example is described as an instance that the potential level applied to the gate electrodes of the NMOS transistor 219, the NMOS transistor 221, and the NMOS transistor 227 is 5 v, the NMOS transistors function as the voltage reducing devices. However, the potential may be such potential as the potential applied to the drain electrodes of the NMOS transistor 215, the NMOS transistor 217, and the NMOS transistor 225 is a potential level that does not destroy the NMOS transistors. For example, the potential may be 6 v or

7 v. However, since an additional circuit for generating this 6 v is needed, the potential is preferably 5 v the same as the power supply potential.

Second Embodiment

Fig. 3 is a circuit diagram illustrating a voltage level shifting circuit 300 of a second embodiment according to the invention.

In the voltage level shifting circuit 300, a reference current source 301 and an NMOS transistor 307 are added to the voltage level shifting circuit 200.

The reference current source 301 and the NMOS transistor 307 are also formed on a semiconductor substrate.

The configuration of a level shift part 203 is different from the configuration of the voltage level shifting circuit of the first embodiment. More specifically, a source electrode of an NMOS transistor 215 and a source electrode of an NMOS transistor 217 are commonly connected to a drain electrode of the NMOS transistor 307. The NMOS transistor 307 is connected between the source electrodes of the NMOS transistor 215 and the NMOS transistor 217 and a ground potential VSS. The NMOS transistor 307 configures a current mirror circuit with an NMOS transistor 305, functioning as a constant current device.

In the second embodiment, a PMOS transistor 211, a PMOS

transistor 213, the NMOS transistor 215, the NMOS transistor 217, and the NMOS transistor 307 configure a current mirror type differential amplifier circuit. The NMOS transistor 307 configures the constant current transistor of this differential amplifier circuit.

Since only a relatively low voltage (about 4 v at the maximum) is applied to the drain electrode of the NMOS transistor 307, this transistor is not required to have high withstand voltage characteristics. Therefore, the transistor is formed in a low withstand voltage area LV as a low withstand voltage transistor.

A reference current source 301 is configured of a constant current source 303 and the NMOS transistor 305. The constant current source 303 is connected between a power supply potential VDD and a drain electrode of the NMOS transistor 305.

The NMOS transistor 305 has a source electrode connected to the ground potential VSS, the drain electrode connected to the constant current source 303, and a gate electrode connected to the drain electrode thereof and a gate electrode of the NMOS transistor 307.

Since only a relatively low voltage (about 4 v at the maximum) is applied to the drain electrode of the NMOS transistor 305, the transistor is not required to have high withstand voltage characteristics. Therefore, the transistor is also formed in the low withstand voltage area LV as a low

withstand voltage transistor. The constant current source 303 is also formed in the low withstand voltage area LV as a low withstand voltage transistor.

Next, the operation of the voltage level shifting circuit 300 of the second embodiment will be described. The operation of the voltage level shifting circuit 300 shown in Fig. 3 is basically similar to the operation of the voltage level shifting circuit 200 shown in Fig. 2. Therefore, only different points will be described in the description below, omitting the overlapping description.

The reference current source 301 generates a predetermined current between the power supply potential VDD and the ground potential VSS. Since the NMOS transistor 305 and the NMOS transistor 307 configure the current mirror circuit, the NMOS transistor 307 functions as the constant current source of the differential amplifier circuit. More specifically, the characteristics of the constant current source 303 and the NMOS transistor 305, which configure the reference current source 301, are set to proper values to set current carried through the level shift part 203. For example, the current carried from the constant current source 303 is reduced, and then the current carried through the level shift part 203 can be further decreased. Consequently, the current consumed by the voltage level shifting circuit can be controlled easily.

As described above, in the voltage level shifting circuit of the second embodiment, the advantage that can easily control the current consumed by the voltage level shifting circuit can be obtained.

What is claimed is:

1. A voltage level shifting circuit comprising:

a first power supply node applied with a first power supply potential level;

a second power supply node applied with a second power supply potential level higher than the first power supply potential level;

a third power supply node applied with a third power supply potential level higher than the second power supply potential level;

a signal input circuit connected between the first power supply node and the second power supply node, the signal input circuit for receiving a signal having the first power supply potential level and the second power supply potential level, and outputting a complementary signal having the first power supply potential level and the second power supply potential level;

a complementary signal input circuit connected to the first power supply node, the complementary signal input circuit having a first electrode connected to the first power supply node, a second electrode, and a gate electrode for receiving the complementary signal, and including a pair of first MOS transistors having a first withstand voltage;

a load circuit connected to the third power supply node, the load circuit having a first electrode connected to the third

power supply node, a second electrode, and a gate electrode, and including a pair of second MOS transistors having a second withstand voltage greater than the first withstand voltage;

a first voltage reducing device connected between the load circuit and the complementary signal input circuit, the first voltage reducing device for preventing a potential exceeding the first withstand voltage from being fed to the complementary signal input circuit;

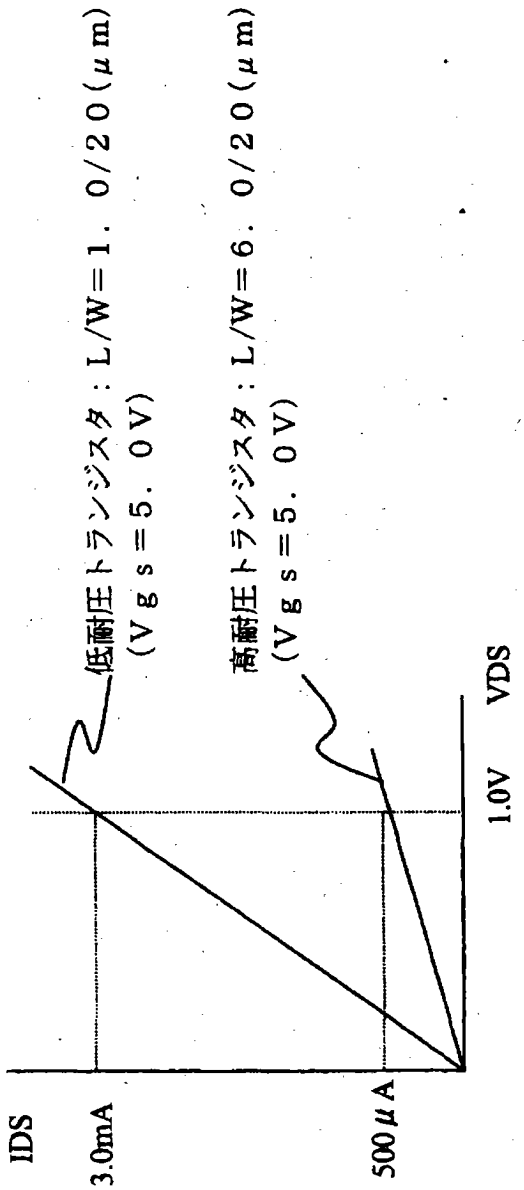
a third MOS transistor connected between the third power supply node and an output node, the third MOS transistor having the second withstand voltage for electrically connecting the third power supply potential node to the output node in response to a potential level outputted from the load circuit;

a fourth MOS transistor connected between the first power supply node and the output node, the fourth MOS transistor having the first withstand voltage for electrically connecting the first power supply potential node to the output node in response to a potential level of one of signals configuring the complementary signal; and

a second voltage reducing device connected between the third MOS transistor and the fourth MOS transistor, the second voltage reducing device for preventing a potential exceeding the first withstand voltage from being fed to the fourth MOS transistor.

ABSTRACT

A voltage level shifting circuit of the invention has a complementary signal input circuit including a pair of MOS transistors having a first withstand voltage for receiving a first logical amplitude, a load circuit including a pair of MOS transistors having a second withstand voltage greater than the first withstand voltage for outputting a second logical amplitude grater than the first logical amplitude, and a first voltage reducing device for preventing a potential exceeding the first withstand voltage from being fed to the complementary signal input circuit. The voltage level shifting circuit further has a third MOS transistor having the second withstand voltage for electrically connecting a third power supply potential node to an output node in response to a potential level outputted from the load circuit, a fourth MOS transistor having the first withstand voltage for electrically connecting a first power supply potential node to the output node in response to a potential level of one of signals configuring the complementary signal, and a second voltage reducing device for preventing a potential exceeding the first withstand voltage from being fed to the fourth MOS transistor.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(Vgs＝5．0V)
高耐圧トランジスタ：L/W＝6．0/20(μm)
(Vgs＝5．0V)
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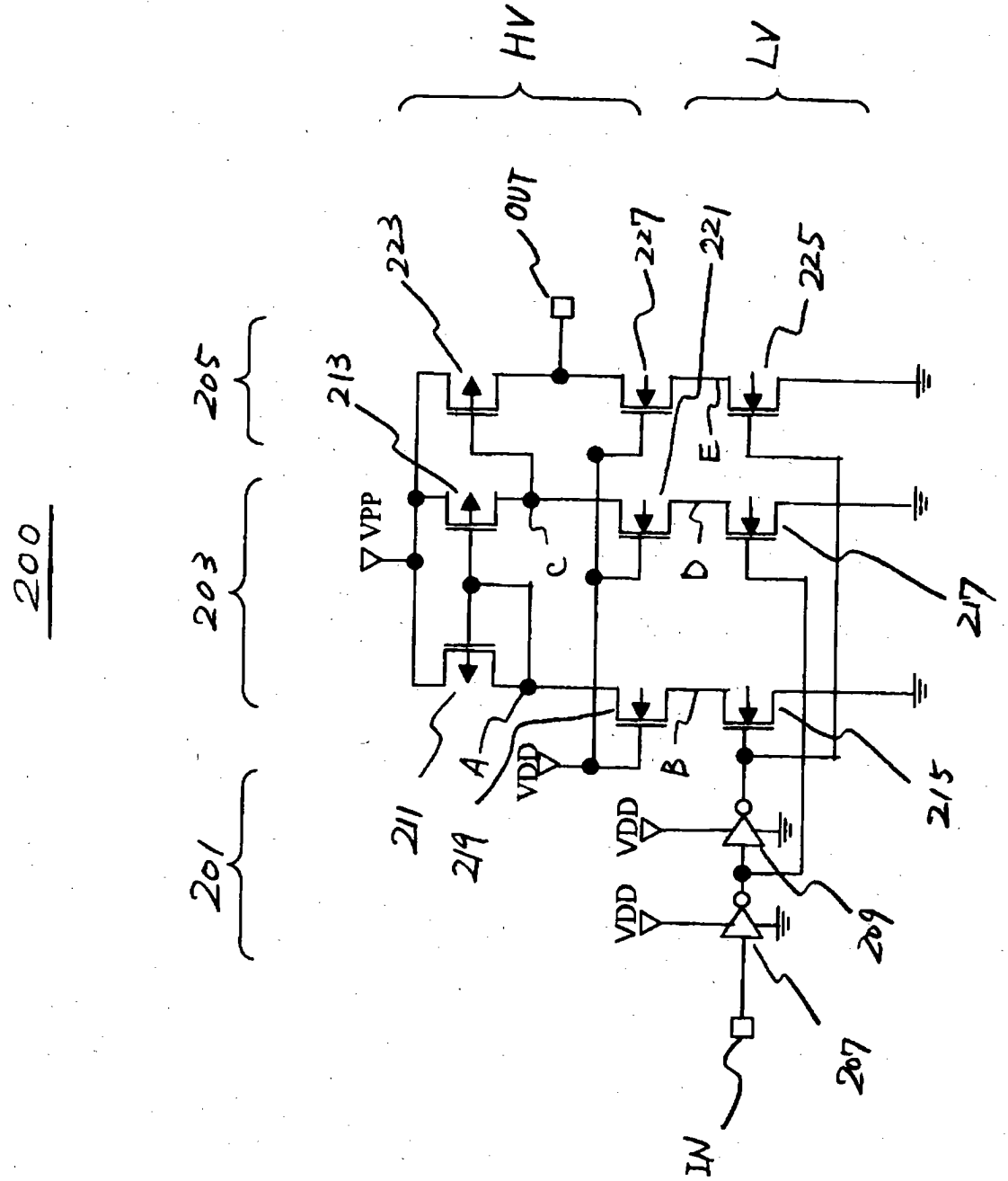
500μA
1.0V
VDS

Fig. 1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203
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211
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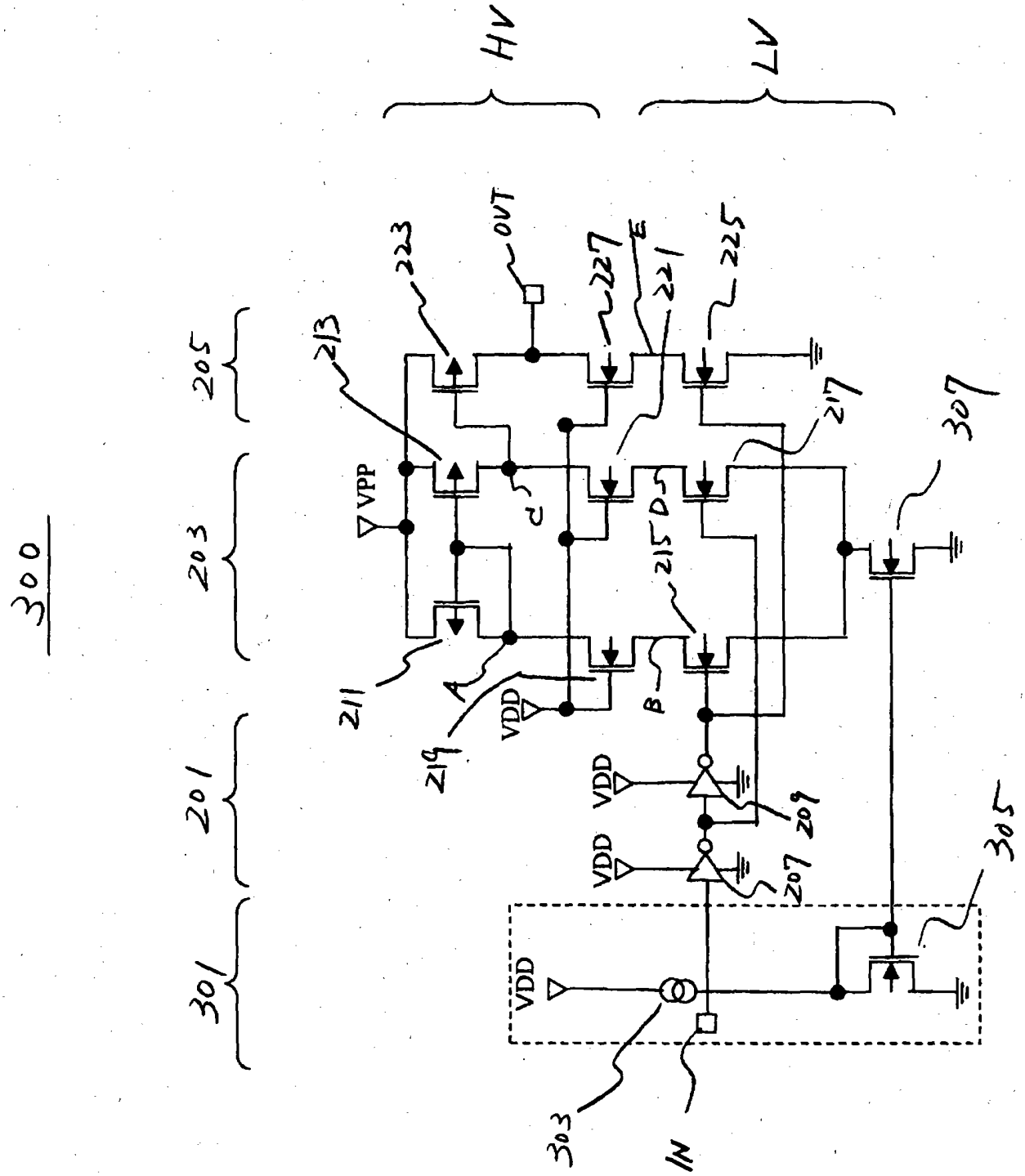
221
223
225
227

Fig. 2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LV
205
203
201
301
213
223
OUT
227
E
221
225
217
307
VPP
C
215
D
211
A
B
219
VDD
VDD
VDD
VDD
209
207
305
303
IN

Fig. 3